LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please cancel claims 1, 4 and 5 without prejudice or disclaimer, and add new claims 8 and 9.

1. (Canceled).

2. (Currently amended) ~~A device according to claim 1,~~ A device comprising:

a receiving shift register for receiving input serial data synchronously with a communication clock signal;

a reception completion determination means coupled to the receiving shift register, the reception completion determination means for also receiving the communication clock signal and for outputting a reception completion signal when detecting that the receiving shift register has received a predetermined number of bits of the serial data based on the communication clock signal;

a pulse-signal generation means for generating a timing pulse signal, which comprises only a predetermined number of timing pulses required for processing the input serial data, in accordance with generation of the reception completion signal by the reception completion determination means; and

a data processing means for processing the input serial data synchronously with the timing pulse signal,

wherein the reception completion determination means includes a counter for counting ~~the~~ a number of input pulses included in the communication clock signal, and for outputting the reception completion signal when a count value of the counter reaches a predetermined number.

3. (Currently amended) ~~A device according to claim 1,~~ A device comprising:

a receiving shift register for receiving input serial data synchronously with a communication clock signal;

a reception completion determination means coupled to the receiving shift register, the reception completion determination means for also receiving the communication clock signal and for outputting a reception completion signal when detecting that the receiving shift register has

received and input a predetermined number of bits of the serial data based on the communication clock signal;

a pulse-signal generation means for generating a timing pulse signal, which comprises only a predetermined number of timing pulses required for processing the input serial data, in accordance with generation of the reception completion signal by the reception completion determination means; and

a data processing means for processing the input serial data synchronously with the timing pulse signal,

wherein the reception completion determination means monitors the serial data for a special bit added to the serial data and outputs the reception completion signal when the special bit is detected.

Claims 4-5 (Canceled).

6. (Currently amended) A device according to claim 2, further comprising:

~~an oscillation unit for generating a system clock signal on the basis of an oscillation command signal~~;

an oscillation control unit for ~~outputting the~~ generating an oscillation command signal in response to receiving an oscillation start signal from the reception completion determination means;

~~a control logic unit~~ a control circuit operating synchronously with the system clock signal and including an oscillation unit in communication with the oscillation control unit, the oscillation unit for oscillating to generate a system clock signal upon receiving the oscillation command signal output from the oscillation control unit;

wherein the oscillation control unit outputs the oscillation command signal functioning as an oscillation start signal when the counter serving as the reception completion determination means has counted a predetermined number of the input pulses included in the communication clock signal.

7. (Currently amended) A device according to ~~claim 4~~ claim 8, further comprising:

a timer included in the control circuit and in communication with the oscillation unit for counting the system clock signal,

wherein the oscillation control unit outputs the oscillation command signal functioning as an oscillation end signal when the timer has measured time of a predetermined length by counting the system clock signal.

8. (New) An electronic control unit comprising:

a receiving shift register for receiving input serial data synchronously with a communication clock signal;

a reception completion determination device coupled to the receiving shift register, the reception completion determination device for also receiving the communication clock signal and for outputting a reception completion signal upon detecting, based on the communication clock signal, that the receiving shift register has received a predetermined number of bits of the serial data;

a pulse-signal generator for generating a timing pulse signal, which includes only a predetermined number of timing pulses required for processing the input serial data, in accordance with generation of the reception completion signal by the reception completion determination means;

a data processor for processing the input serial data synchronously with the timing pulse signal, the data processor including an oscillation control unit for generating an oscillation command signal in response to receiving the reception completion signal from the reception completion determination device; and

a control circuit for operating synchronously with the system clock signal and including an oscillation unit in communication with the oscillation control unit, the oscillation unit for oscillating to generate a system clock signal upon receiving the oscillation command signal from the oscillation control unit.

9. (New) The electronic control unit according to claim 8, wherein the oscillation control unit outputs the oscillation command signal based on command data corresponding to the serial data.